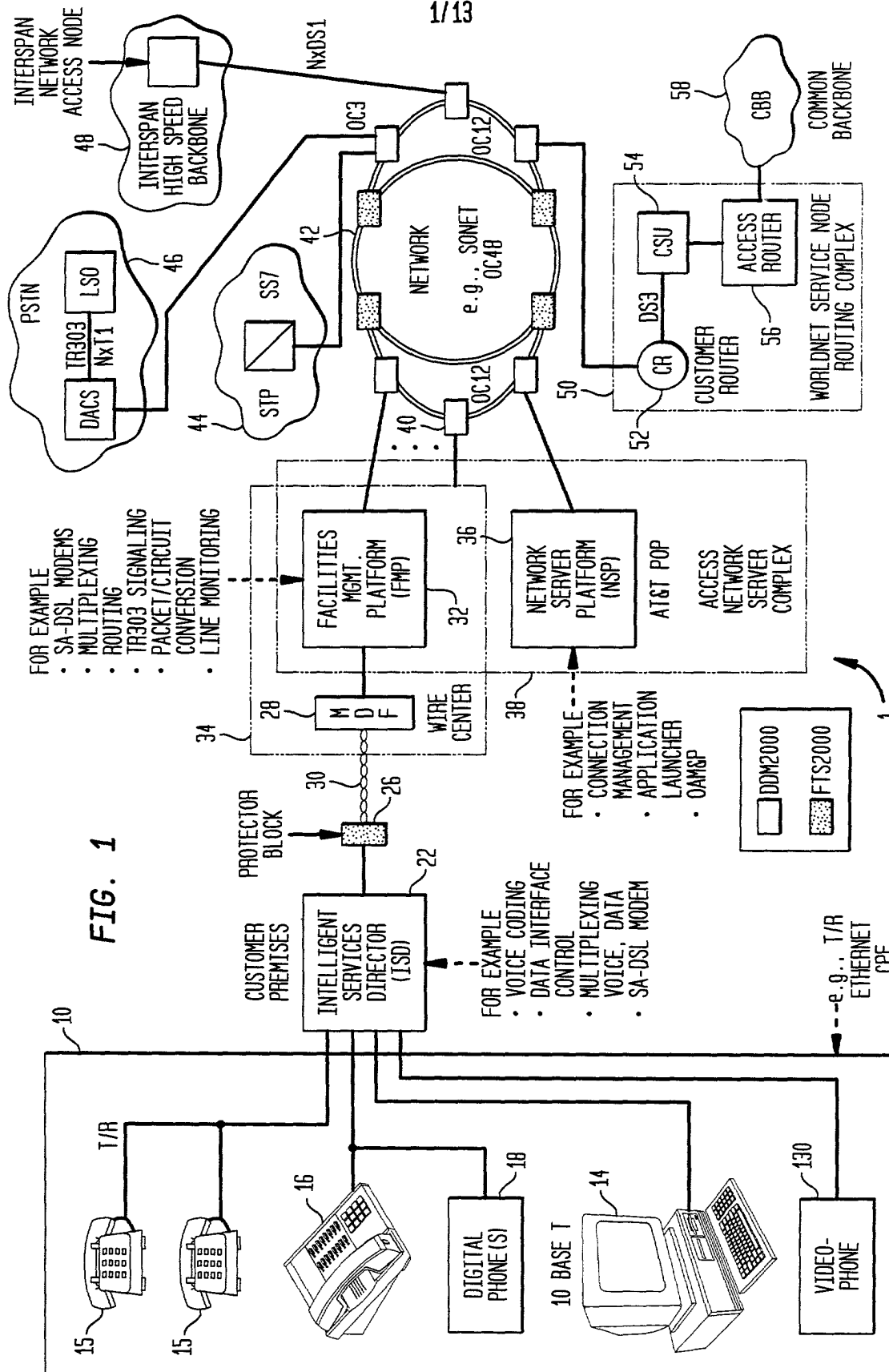
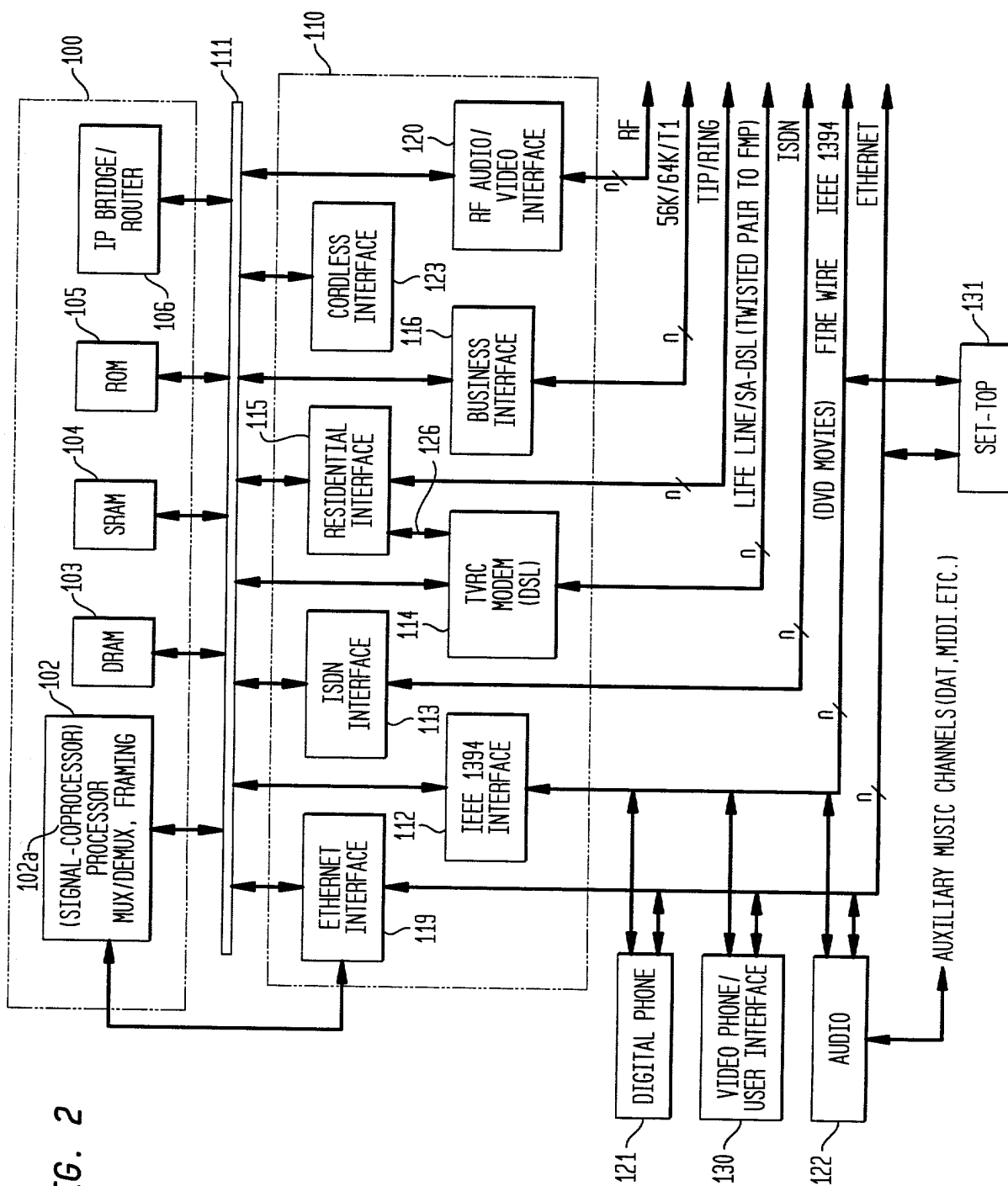


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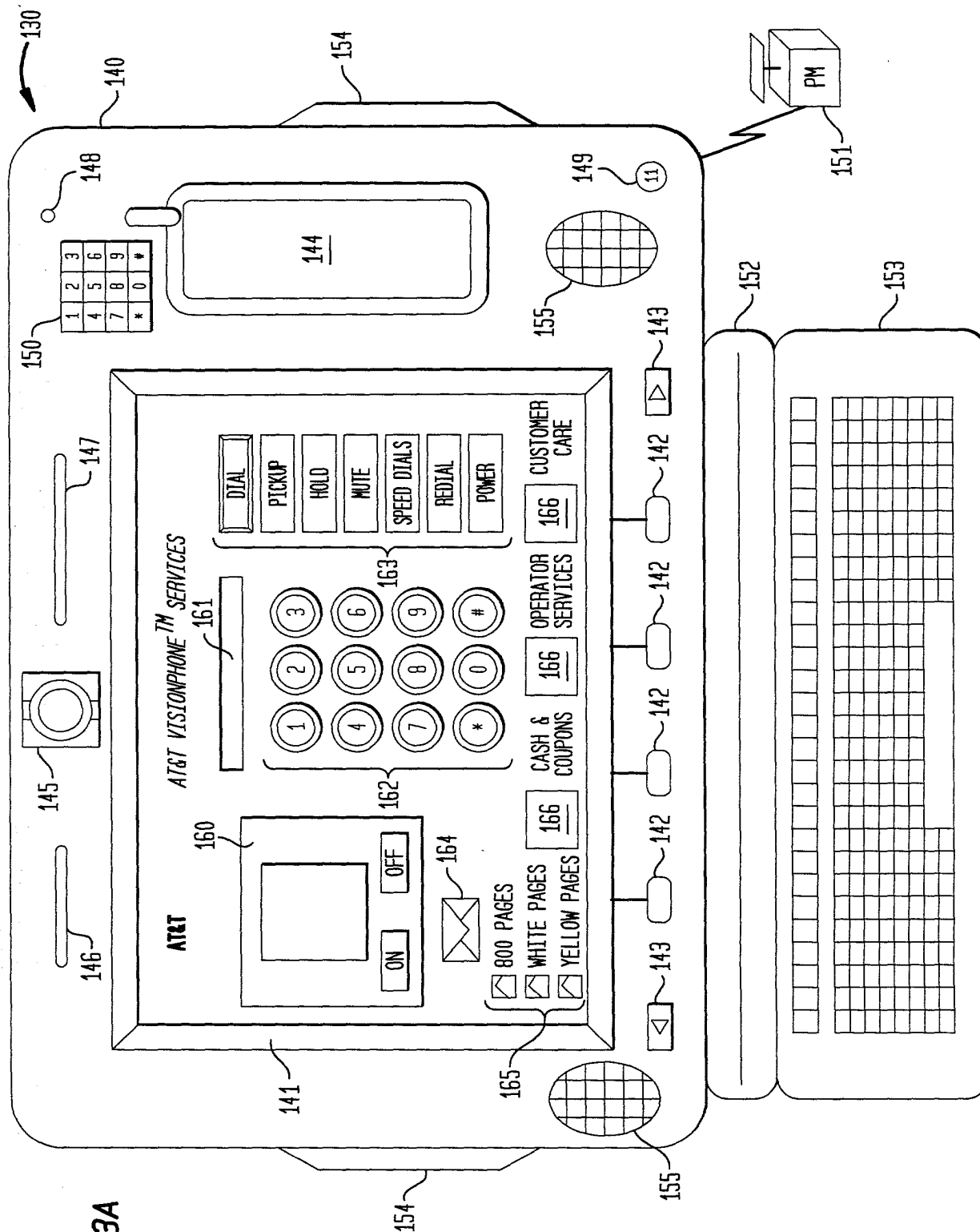


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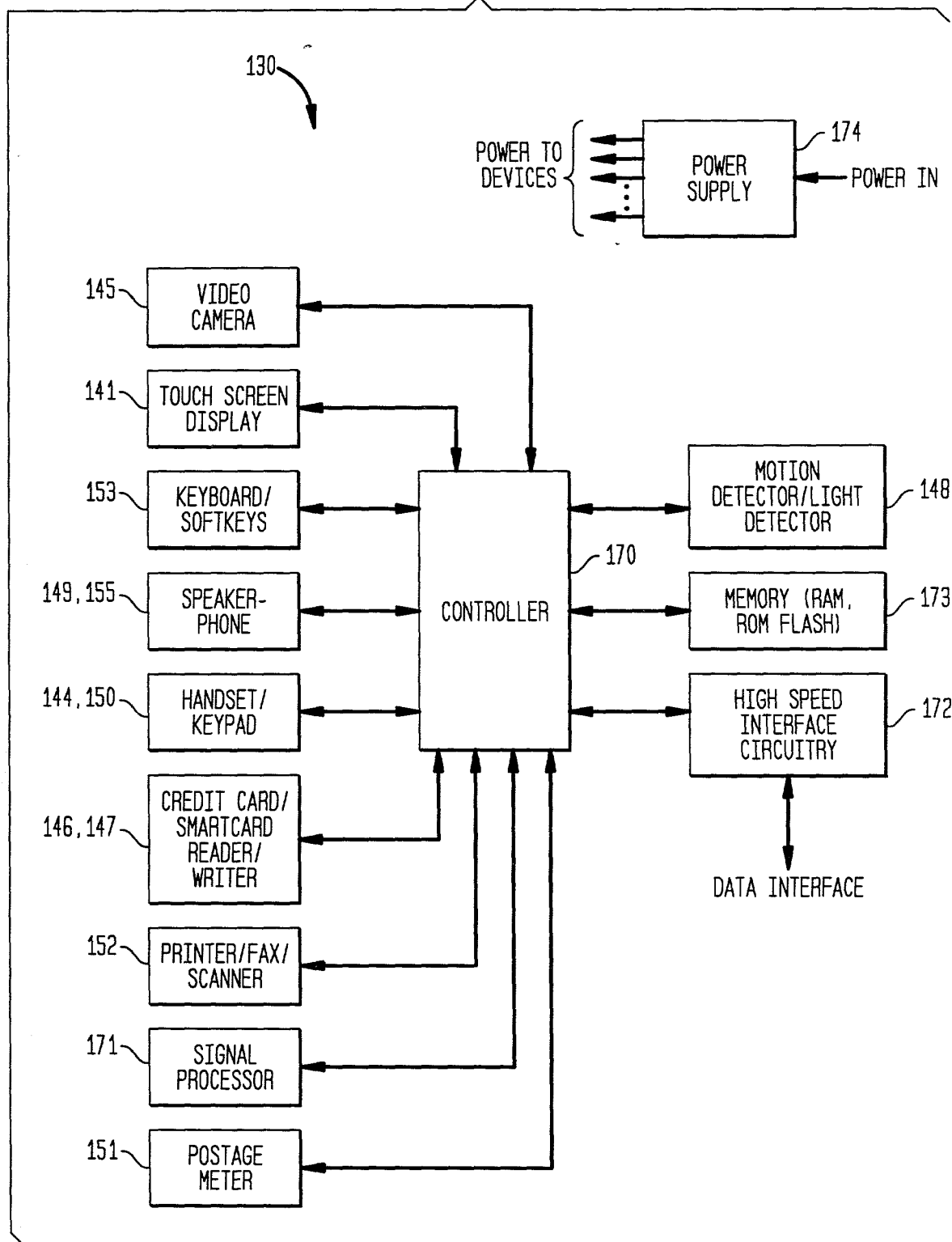
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FIG. 3A



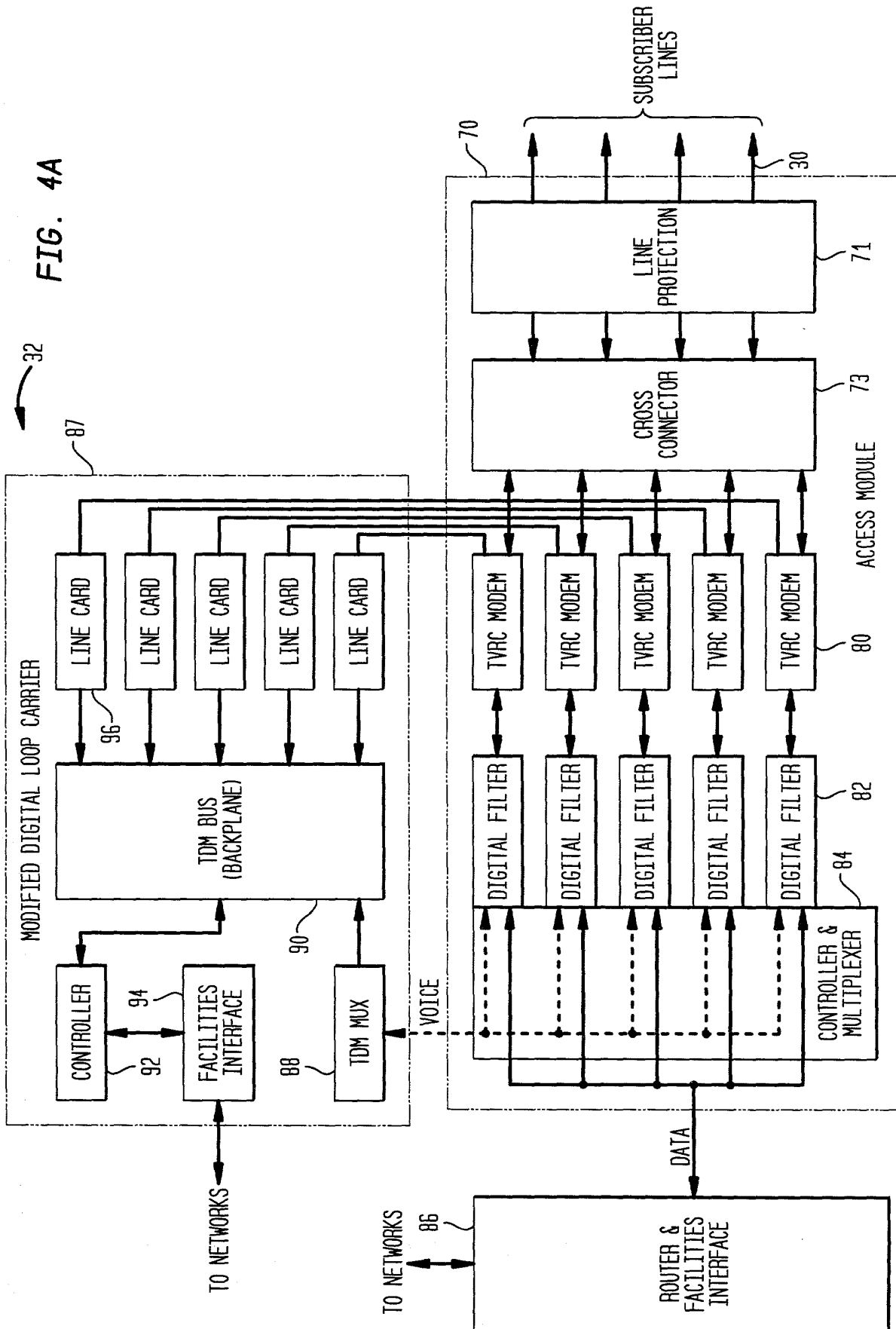
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FIG. 3B



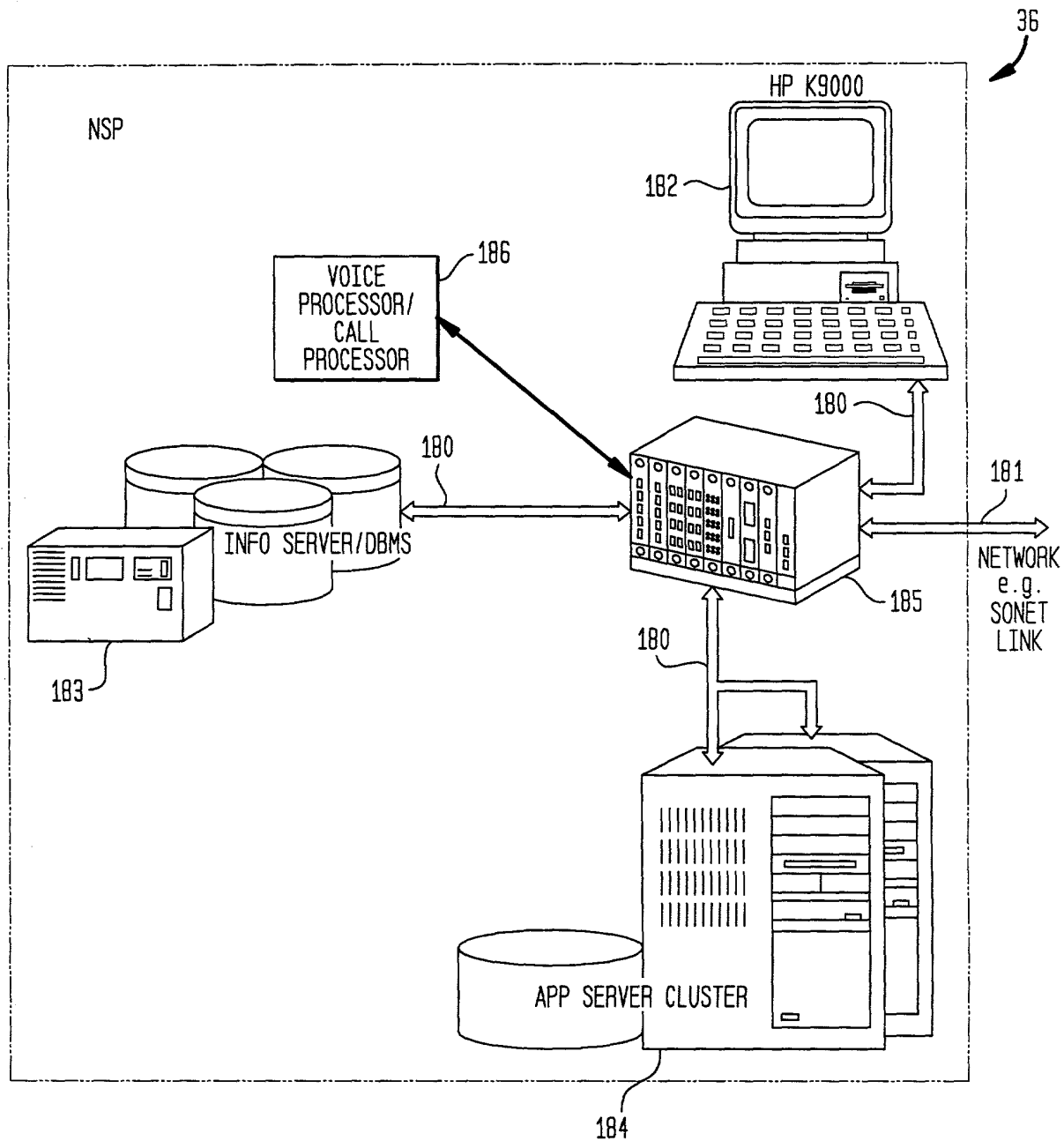
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FIG. 4A

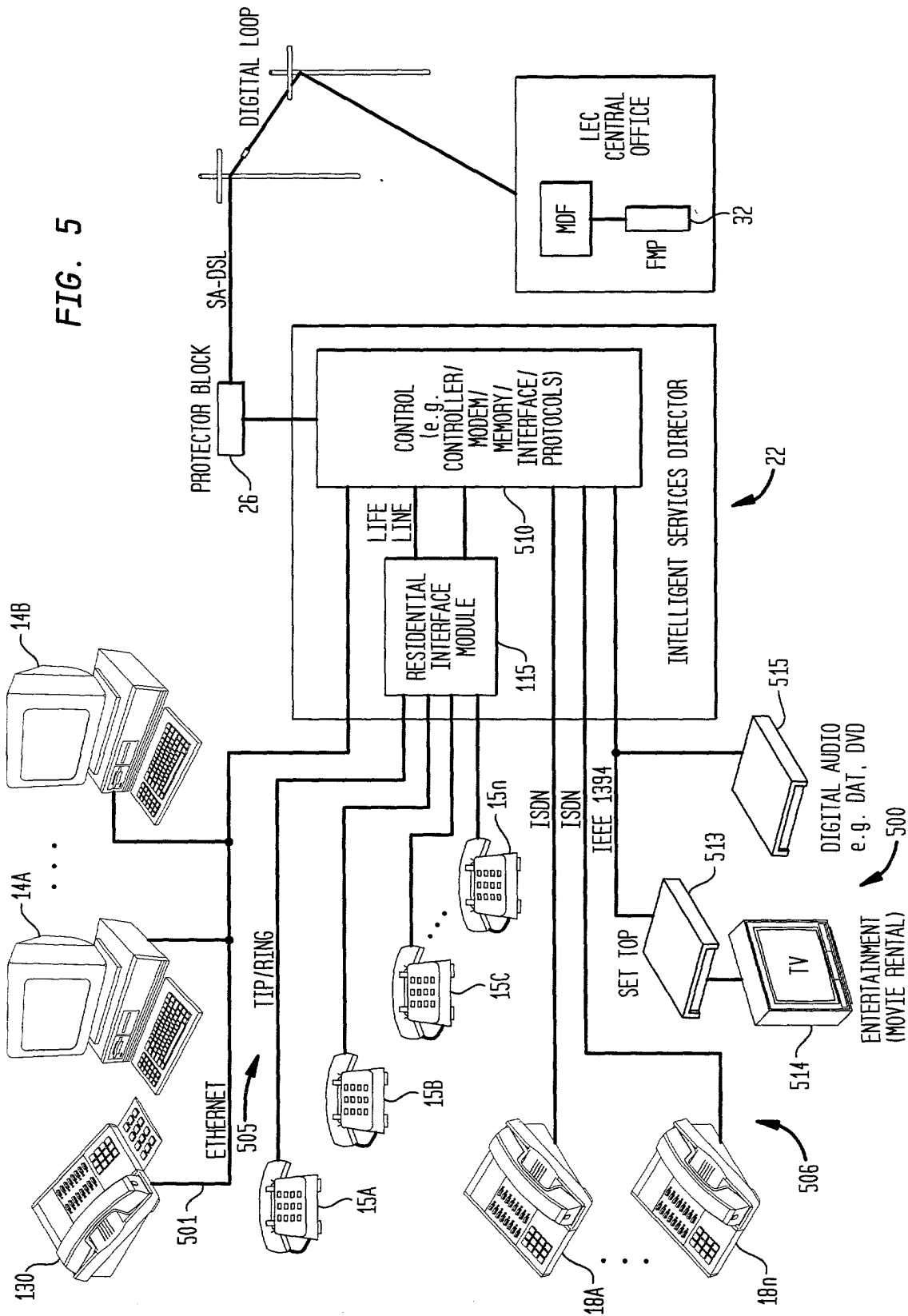


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FIG. 4B



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FIG. 6A

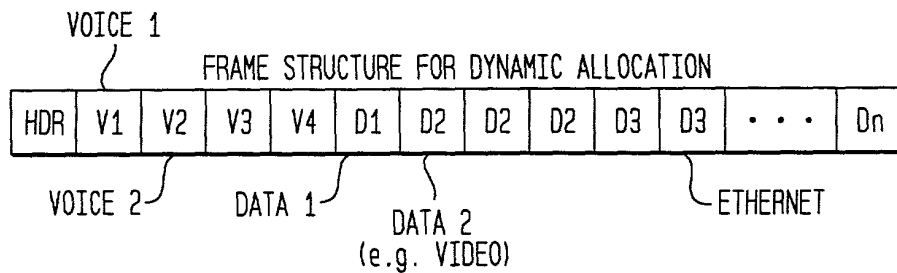
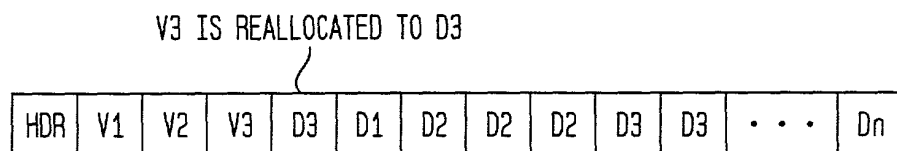


FIG. 6B



HDR - HEADER CONTAINING CONTROL INFORMATION
IN THIS EXAMPLE, EACH SLOT IS A 64 Kbps TIME SLOT

FIG. 7A

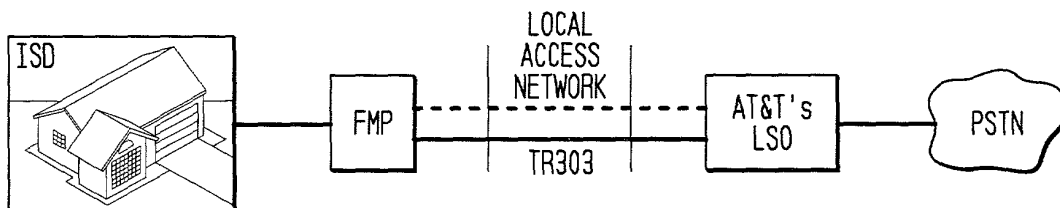
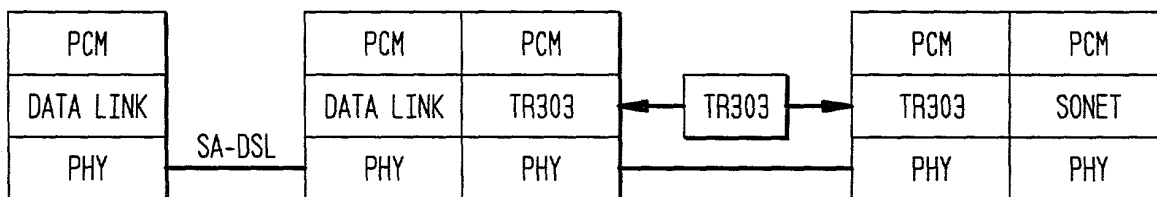


FIG. 7B



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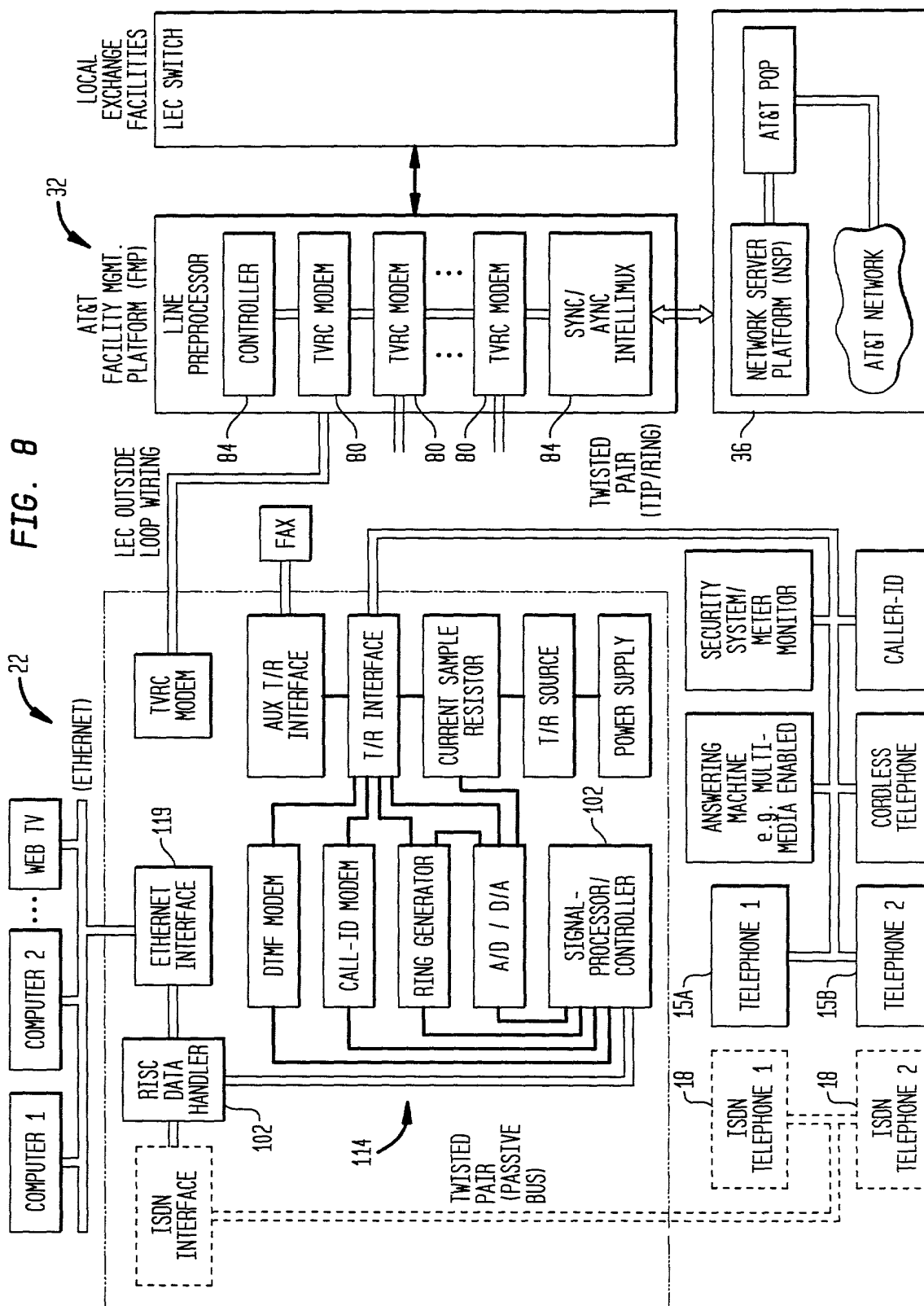
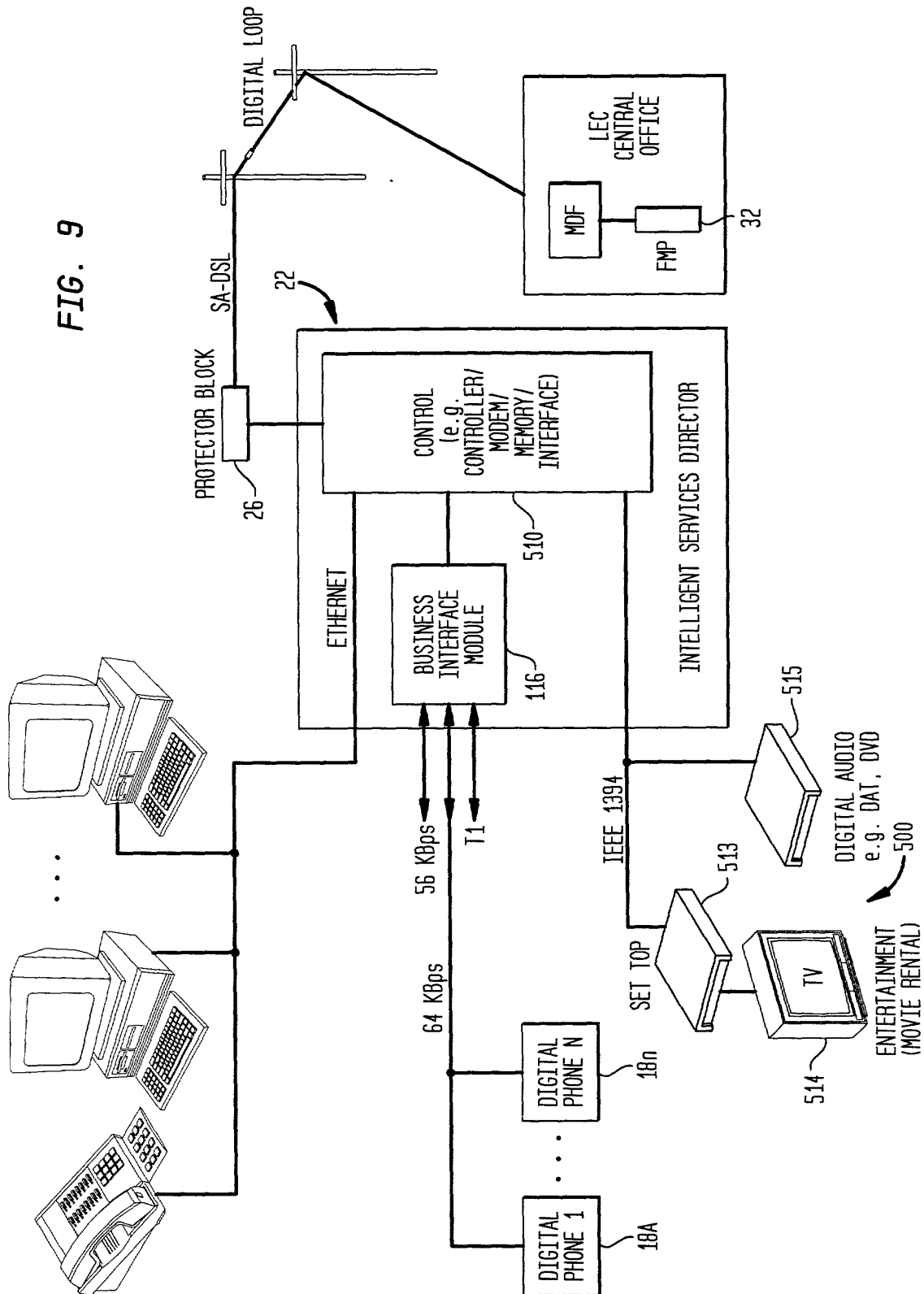
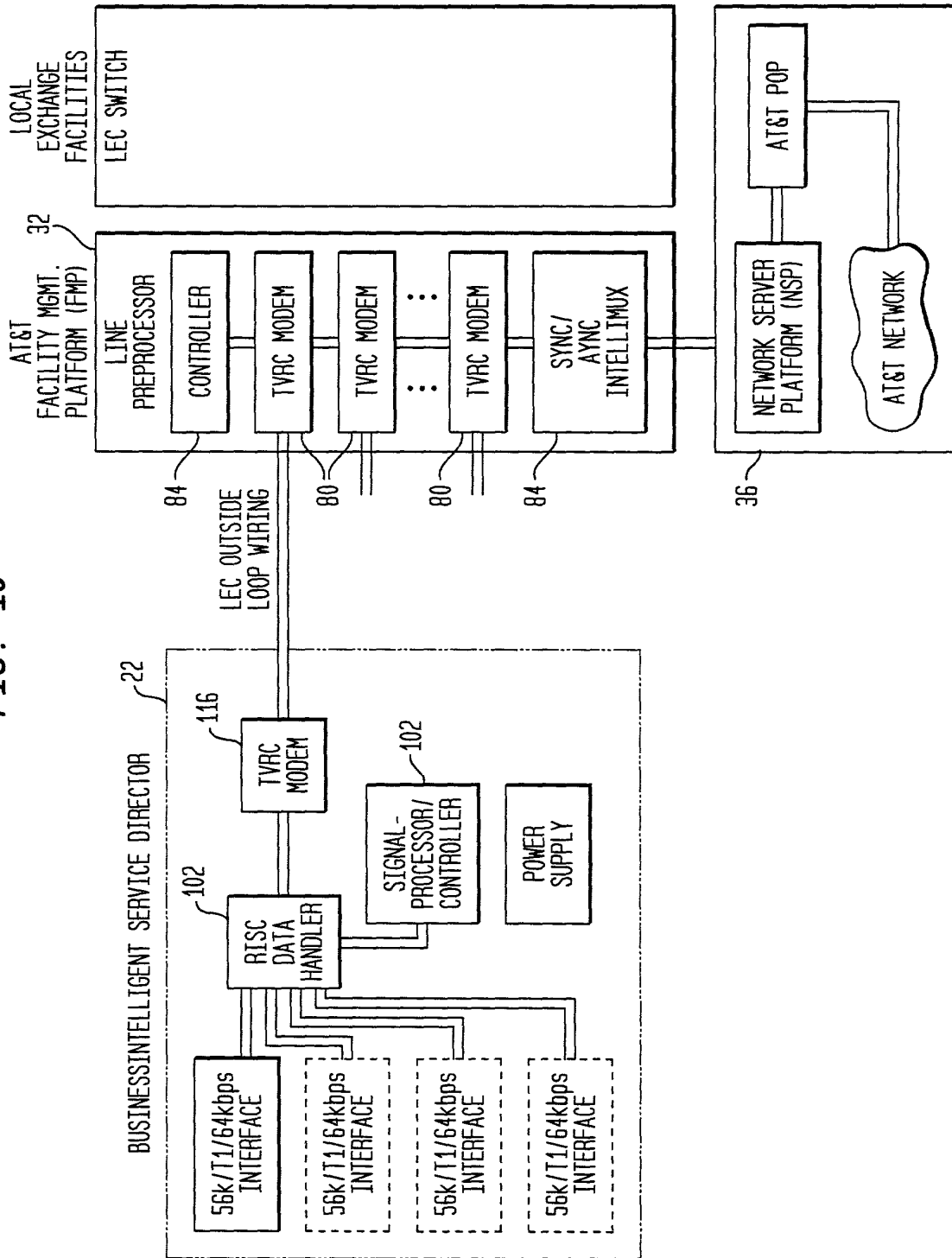


FIG. 9



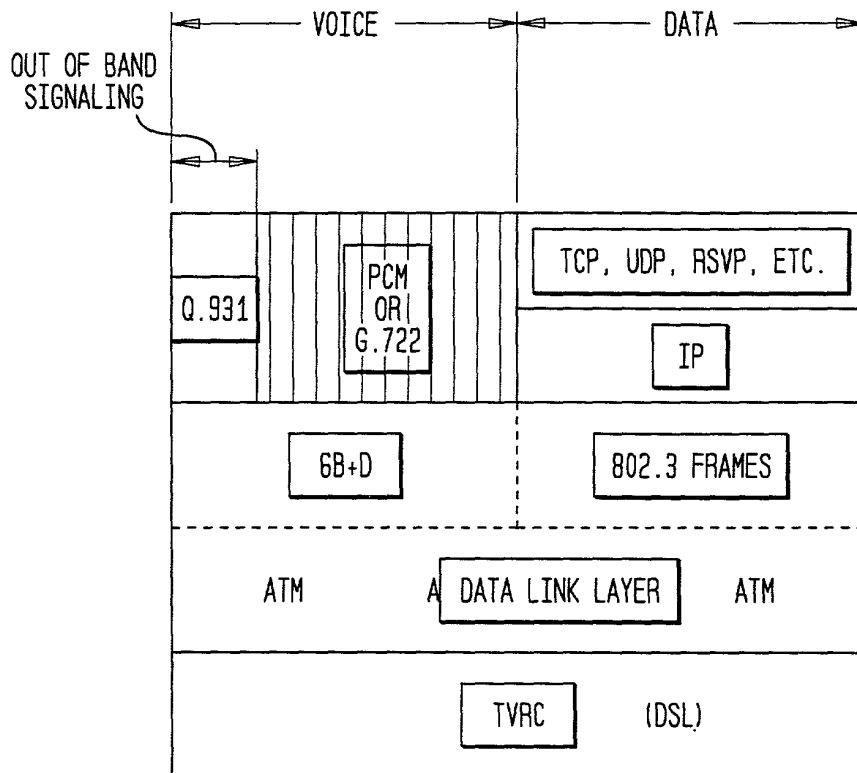
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FIG. 10



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FIG. 11



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FIG. 12

